January 31, 2007

Bolko von Roedern
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

Re: NREL Subcontract #ADJ-1-30630-12
D.5.9

Dear Bolko,

This report covers research conducted at the Institute of Energy Conversion (IEC) for the period of October 16, 2006 to November 15, 2006, under the subject subcontract. The report highlights progress and results obtained under Task 1 (CdTe-based solar cells).

Task 1 - CdTe-based Solar Cells

In terms of the ultimate device performance achievable on cells using commercially available soda lime substrates, we have attained V_{OC} up to 850 mV, which is comparable to the best V_{OC} obtained on borosilicate glass. However, high V_{OC} and FF are infrequently obtained with routine baseline processing. A study is warranted to determine the effects of glass handling and cleaning and buffer layer formation on the grain structure and variability in performance of the CdTe devices. Statistical analysis of the device performance of more than 450 VT devices using the baseline process revealed a V_{OC} distribution with a sharp maximum at 800 mV and excursions to 850 mV. The effort to demonstrably improve V_{OC} and to fabricate cells with ultra-thin absorber layers will require a tighter baseline distribution. Due to the combination of superstrate configuration and high processing temperatures used for VT CdTe solar cells, uncontrolled impurities originating in the glass/SnO_2 and its handling can become trapped in the structure and critically affect junction quality, in which case the intrinsic buffer layer may serve as a diffusion barrier as well as an electronic circuit element. The role of the Ga_2O_3 in mitigating effects from the SnO_2 is demonstrated in Table I for cells made from a single VT deposition with and without Ga_2O_3 and CdS in the window side of the device.

Table I. Device results for VT CdTe solar cells on TEC15 soda-lime glass/SnO_2 substrates.

Device	Window Layer	V_{OC} (mV)	FF (%)
VT213.1	SnO_2 (no Ga_2O_3, no CdS)	159	28.4
VT213.2	SnO_2/Ga_2O_3 (no CdS)	432	44.1
VT213.3	SnO_2/Ga_2O_3/CdS	767	60.0

The cells without Ga_2O_3 and CdS (VT 213.1) exhibit severe electrical shunt behavior. This is eliminated by the addition of the Ga_2O_3 (VT213.2); however, the diodes are soft and have low V_{OC}. The critical role of the Ga_2O_3 is demonstrated by the fact that all 8 cells from VT213.1 were severely shunted while none of the 8 cells on VT213.2 were shunted.

The selected experimental approach examined the effects on CdTe films and devices of the preparation of the TEC 15 glass/SnO_2 prior to the deposition of the CdTe film. This included the cleaning of the substrate, pre-baking of the glass/SnO_2 in air at 550°C, the deposition of a 100-300 Å Ga layer and its subsequent oxidation time. The pre-bake step was evaluated as a means to oxidize carbonaceous and metallic residues from glass cutting and handling. It is anticipated that although the particular results are lab and process-specific, more general conclusions and a path for refining glass/TCO handling which can tighten the V_{OC} distribution will be found, so that advancements in ultimate V_{OC} can be achieved.

All samples were cleaned using our standard Crest cleaning system that consists of a hot ultrasonic soap (Liquinox) wash, followed by a hot ultrasonic water rinse and forced hot air drying. The processing of the substrate after this point was varied to compare bake time for glass preparation and Ga oxidation, Ga deposition time, and rinse water purity (Table II). The rinse was performed after the pre-bake and Ga oxidation steps. The pre-bake was done in air at 550°C for the indicated time. The oxidation of the Ga was again done at 550°C for the time shown. Analysis consisted of surface chemical assays using XPS, optical microscopy to examine the effect on CdTe film morphology, and device performance. Following the oxidation step, all the samples received our baseline CdS and CdTe film deposition. Cells were processed with the established baseline vapor $CdCl_2$ treatment for 2 minutes at 480°C and aniline treatment, with Cu/Ni contacts.

Table II. Sequential Glass/TCO/HR processing steps used for VT CdTe devices.

Run Number	Pre-Bake Time (min)	ED Ga Dep Time (min)	Ga Oxidation Time (min)	Rinse Water
242	75	none	none	cold Nanopure
243	75	10	75	cold Nanopure
244	none	10	75	cold Nanopure
247	none	10	80	cold Nanopure
248	15	15	15	cold Nanopure
249	15	10	15	cold Nanopure
251	15	20	15	Hot Tap
252	15	15	15	Hot Tap
267	none	none	75	cold Nanopure

Optical micrographs of the resulting CdTe films show a wide variation in grain size for films of constant thickness (~7 microns) depending on the HR layer processing. Figure 1 compares films deposited onto CdS-coated substrates with no Ga_2O_3 HR layer(VT 242) and with 30 nm Ga_2O_3, formed by oxidation of Ga films deposited either by sputtering (VT 197), electron beam evaporation (VT 267) or electrodeposition (VT 244). All films exhibit faceted grain morphology with evidence of thermal grooving on the large faces and bimodal grain size distribution, with the largest grains found for the film with e-beam and electrodeposited Ga.

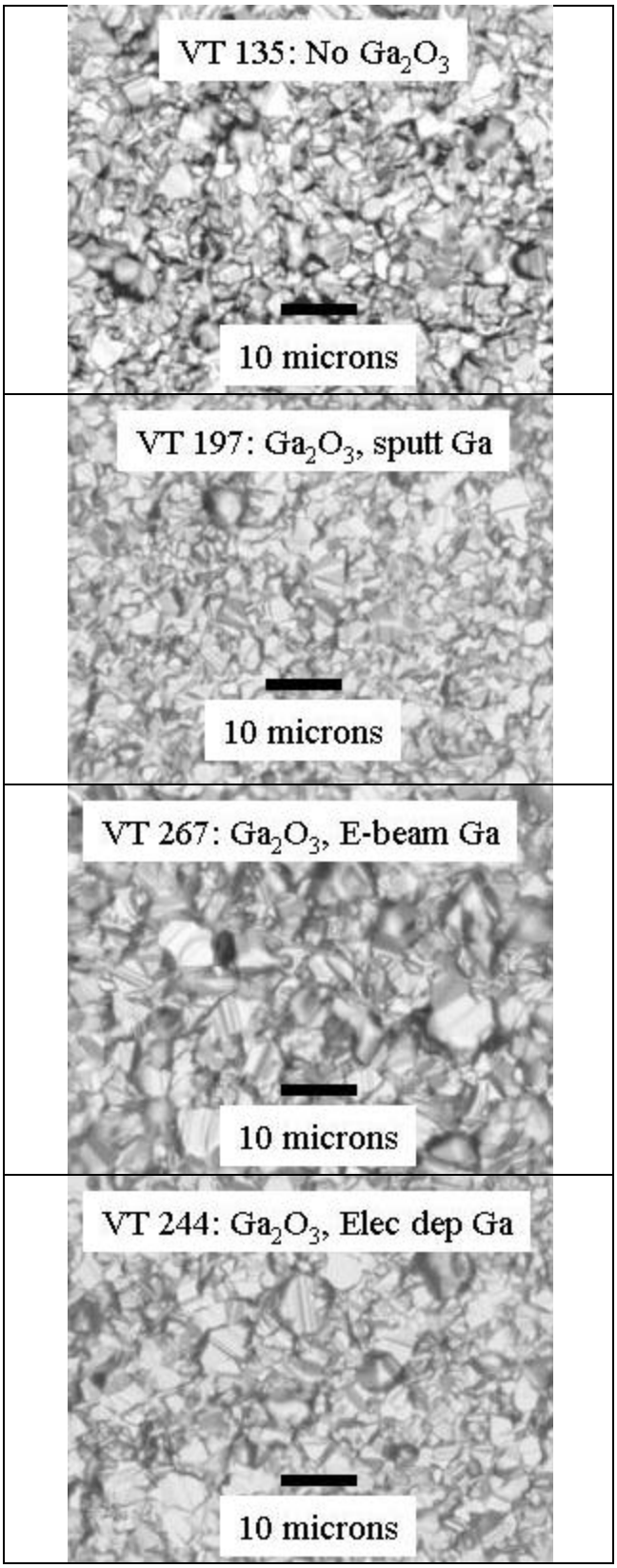

Figure 1. Optical micrographs of VT CdTe film surfaces for films deposited on substrates with no Ga_2O_3 (top) and with Ga_2O_3 made by oxidation of different Ga precursors. Cells with efficiency > 10% were achieved on all configurations shown in Figure 1, but the highest V_{OC} 's were obtained for cells with Ga_2O_3. To accommodate high batch throughput, electrodeposition was selected as the standard method for making the Ga precursors.

Pre-baking the glass/TCO was found to produce larger CdTe grains than on films without Ga_2O_3 but yielded smaller, more densely pack grains on films with electrodeposited Ga precursors compared to the other deposition methods. It was found that increasing the Ga oxidation time, however, increased the overall grain size and decreased grain size uniformity. This suggests a mechanism for CdTe grain nucleation linked to diffusion of species from the glass/TCO. Increasing the oxidation time simply increases the concentration of these impurities through the Ga_2O_3, as suggested by a dramatic increase in the number of larger grains and the bimodal distribution (Figure 2).

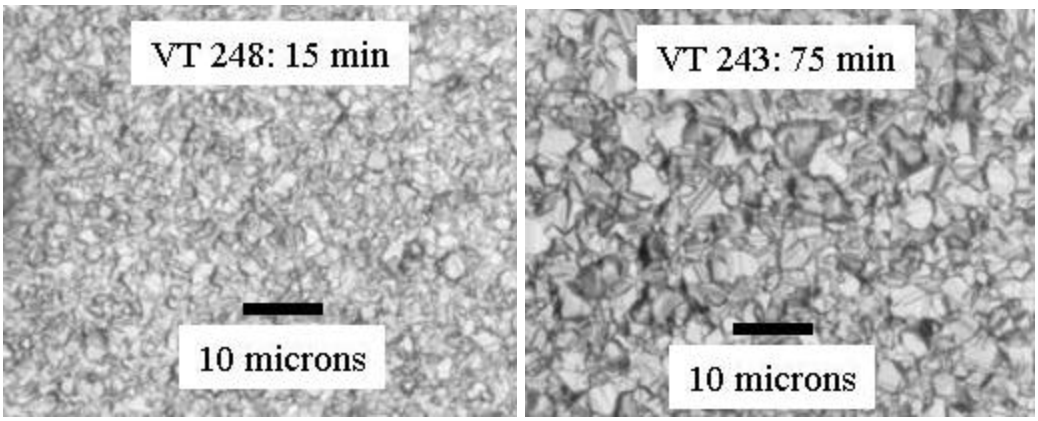

Figure 2. Optical micrographs of CdTe surface comparing the effect of Ga oxidation time using electrodeposited Ga; both samples were pre-baked prior to Ga deposition.

Varying the purity of the final water rinse step prior to CdS growth (i.e., after the Ga oxidation) was also found to have a strong effect on the CdTe grain size and distribution. The standard method, used in the above examples, utilized room temperature Nanopure water rinse. Using a hot tap water rinse between steps negated the effects of the pre-bake and buffer layer, resulting in CdTe films with uniform, large grain morphology (Figure 3).

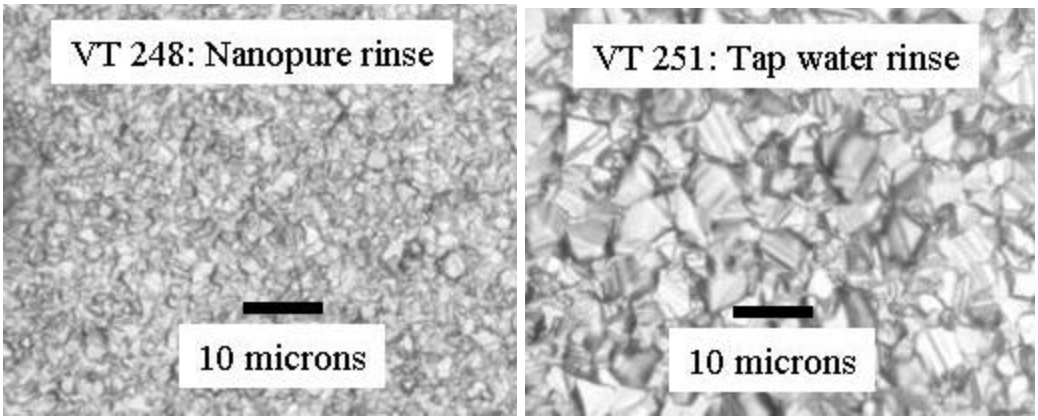

Figure 3. Optical micrographs of CdTe surface comparing the effect of rinse water purity.

XPS analysis was carried out for glass/TCO samples in as-received, rinsed and thermal annealed conditions (Table III). Impurities such as Cu and V were found introduced following the rinse step. The Ce found on the SnO_2 surface originates in the glass but the Cu and V are introduced during the rinsing step. Thermal annealing lowered the signals, likely due to diffusion into the

TCO. It is planned to repeat the XPS survey on samples coated with Ga_2O_3 after different anneal times and to perform SIMS depth profile analysis for trace impurities.

Table III. XPS analysis for glass/TCO surface for the given processing.

Sample Set	Process step	Surface Elements
2	As Received	Sn, O, Ce, C
2	+ tap water rinse	same + Cu, V
2	+ 550°C air HT	same but Cu, V levels reduced
1	tap water rinse	Sn, O, Ce, Cu, V, C
1	+ 550°C air HT	same but Cu, V levels reduced

Table IV compares the device results obtained for the different bake and rinse variations listed in Table II. The sample with the highest V_{OC} and efficiency (VT 249) was processed with electrodeposited Ga and the shortest overall thermal treatment (15 minute pre-bake and 15 minute Ga oxidation) and Nanopure water rinsing. The highest FF was obtained for samples with a long, 75 minute, pre-bake (VT 242 and VT 243), independent of the presence of Ga_2O_3. In the case without Ga_2O_3, the V_{OC} was < 700 mV. Hot tap water rinsing likewise produced low V_{OC} and was found to introduce impurities, which affect the nucleation of the CdTe film. The lowest FF was obtained for the sample with no pre-bake (VT 244) and for the sample with the tap water rinse (VT 252). Samples VT 251 and VT 252, both rinsed with tap water, had slightly different Ga thickness, attained by varying the Ga deposition time. The sample with thicker Ga, VT 251, exhibited higher V_{OC} and FF, suggesting that the Ga oxide serves as a diffusion barrier to some impurities, in this case, arising from the tap water rinse.

Table IV. Device results for samples of Table II.

Run Number	Ga Type	V_{OC} (mV)	FF (%)	Eff (%)
242	None	650	75	12.5
243	ED	730	75	13.3
244	ED	760	65	12.2
248	ED	750	70	12.8
249	ED	800	72	14.1
251	ED	700	66	10.0
252	ED	600	52	7.0
267	E-beam	760	58	10.4

The results allow the following conclusions to be drawn:

1) TCO rinsing and thermal treatment can add and redistribute impurities, affecting CdTe nucleation and device V_{OC} and FF;
2) Ga_2O_3 is needed for high V_{OC} (see Table I and compare VT 242 and VT 243 in Table IV);
3) Ga_2O_3 may serve as a diffusion barrier (compare VT 251 with VT 252);
4) Long pre-bake (VT 243) improves FF but reduces V_{OC} (compare with VT 244);
5) Replacing Nanopure rinse with tap water rinse reduces V_{OC} and FF (VT 248, VT 249, VT 251, VT 252), suggesting strong sensitivity to rinse steps.

Best regards,

Robert W. Birkmire
Director

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